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Low power Arithmetic Logic Unit Design for IoT applications

N.Naveen Kumar[1], B.Lakshmi Prasanna[2], V.Harathi[3], R.Somesh[4], E.C.Deepthi[5], G.Chinna[6]
*[1]Research Supervisor, Assistant Professor, Dept.of ECE, ALTS, Anantapuramu
[2,3,4,5,6] UG Scholoar, Dept.of ECE, ALTS, Anantapuramu

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ABSTRACT

The increasing adoption of Internet of Things (IoT) technologies necessitates energy-efficient and optimized processor architectures. A fundamental unit within these architectures is the Arithmetic Logic Unit (ALU), which plays a pivotal role in computational operations and overall system performance. This study introduces an enhanced ALU design incorporating a hybrid approach of clock gating and gray coding techniques, termed CGGC. By leveraging these methods, unnecessary switching activities are minimized, leading to lower power consumption and improved hardware efficiency. The design was developed using Verilog and validated on the Vivado 16 simulation platform. Experimental findings indicate an 18% reduction in Look-Up Table (LUT) utilization, demonstrating significant resource optimization for IoT-based applications. The proposed CGGC architecture ensures a synergy between computational efficiency and power conservation, making it a viable candidate for low-power embedded systems. Future research will focus on refining power optimization strategies and implementing the architecture on FPGA platforms for practical validation.

Keywords: IoT Processor Architecture, Arithmetic Logic Unit (ALU), Clock Gating, Gray Coding, Low-Power Design, Resource Optimization, Vivado Simulation.

I. INTRODUCTION

The evolution of microprocessors began with the Intel 4004, the first 4-bit semiconductor processor developed in 1971 by Intel. Over the decades, processing power has significantly advanced, with modern CPUs and controllers now operating at 64-bit and beyond, achieving clock frequencies in the MHz to GHz range. This progress has been largely driven by CMOS technology, enabling higher transistor densities on silicon wafers. However, this miniaturization leads to increased power consumption and energy inefficiency, necessitating research into low-power architectures.

To mitigate excessive power usage, various techniques have been explored, including clock gating, block devices, and heartbeat mechanisms. Clock gating, a widely used power-saving approach, is categorized into three types: latch-based, flip-flop-based, and latchless clock gating. Additionally, reducing energy leakage is essential, as it directly correlates with the number of active processing sites. Two optimization strategies have been introduced to refine timing measurements, particularly for wearable technology applications.

II. EXISTING METHOD

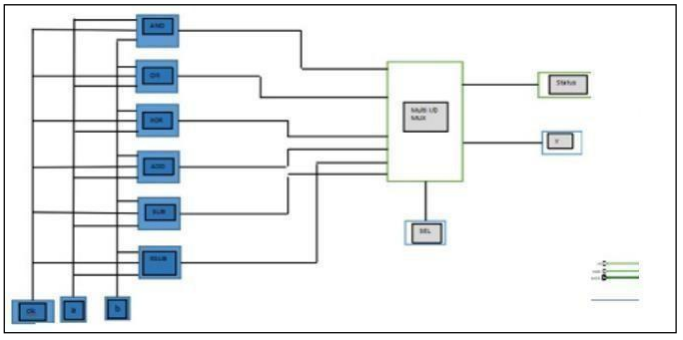

Fig.1: Block diagram of normal ALU

Conceptually, a traditional ALU operates like a versatile Swiss Army knife of digital computation. It comprises specialized functional units, each dedicated to performing a specific arithmetic or logical operation, such as addition, subtraction, AND, OR, XOR, and more. Imagine these units as individual tools, each ready to tackle a particular task. To select the desired operation, a

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control signal, often termed "SEL", acts as the maestro, directing the output of the appropriate functional unit to a multiplexer, which acts as the final gatekeeper, outputting the chosen result.

III. PROPOSED METHOD

A. Clock Gating: This research examines power dissipation in Arithmetic Logic Units (ALUs), which occurs in two forms: dynamic power dissipation when the ALU is operational and static power dissipation when it is inactive. A substantial portion of energy consumption arises from the switching activity of input signals. To enhance dynamic power efficiency, precise clock control mechanisms are essential. By temporarily deactivating unused modules or shutting down inactive components, unnecessary power usage can be significantly reduced. One effective method to achieve this is clock gating, which restricts data updates to only the essential units whose outputs are required. A gated clock is implemented using a D flip-flop, where the clock signal synchronizes all flip-flops simultaneously. The stored values remain unchanged unless the selection signal is enabled, ensuring that data registers update only when necessary. The "EN" signal regulates the clock input, generating a gated clock signal that enhances power efficiency by reducing unnecessary switching activities.

B. Gray Coding: Gray coding, also referred to as Gray binary code or the reflected binary code, is an alternative numeral system that differs from conventional binary representation. It is specifically designed to simplify circuit operations and minimize errors by ensuring that consecutive values vary by only a single bit. This unique property makes Gray coding particularly advantageous in communication systems and rotary encoders, where preventing large transitions between successive values is critical. Unlike standard binary numbering, which allows for significant changes between adjacent numbers, Gray coding ensures smooth transitions, thereby reducing the chances of misinterpretation. This feature makes it highly effective for error detection and correction, enhancing overall system reliability. Due to its ability to maintain data integrity and improve precision, Gray coding plays a crucial role in various digital applications, ensuring efficiency and accuracy in electronic and computational systems.

C. Modified ALU: The 8-bit ALU architecture comprises two functional components, "a" and "b", along with a 4-bit selection input ("SEL") that dictates the operation to be executed. The ALU supports a variety of arithmetic and logical operations, including clear, return, complement, increment, decrement, and addition, among others. Since both inputs are 8-bit values, certain operations may generate results exceeding this bit-width. The final output, "Y", consists of 16 elements, storing the computed results efficiently.

Operations	Opcode
Clear	0000
Return b	0001
Compliment b	0010
Return a	0011
Increment	0101
Decrement	0110
Left Shift	0111
Add	1000
Subtract	1001
Add with carry	1010
Subtract with carry	1011
AND	1100
OR	1101
XOR	1110
XNOR	1111

Table.1: Logical and Arithmetic operations

One of the key challenges in ALU design is excessive switching activity, which arises when the clock signal remains active across all operational blocks, even when some are not in use. This unnecessary activation leads to increased power consumption due to continuous switching at idle components. Given that the ALU performs only a single operation at a time, power efficiency can be significantly improved by disabling the clock for inactive modules, thereby reducing energy wastage.

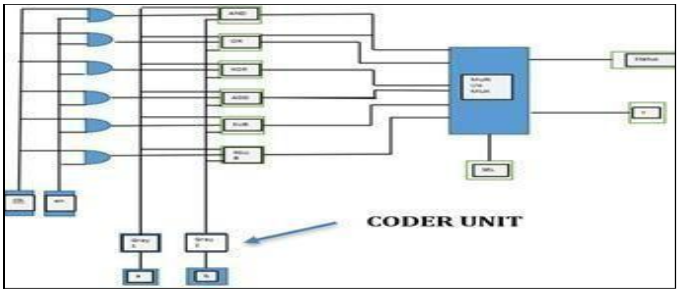

Fig.2: Block diagram of modified ALU

To enhance energy efficiency, the proposed ALU design integrates Clock Gating and Gray Coding (CGGC) techniques. This approach ensures that power is allocated only to the functional blocks involved in the selected operation, minimizing unnecessary switching and optimizing overall performance. A comparative analysis of the conventional and optimized architectures

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highlights significant improvements in power efficiency and resource utilization.

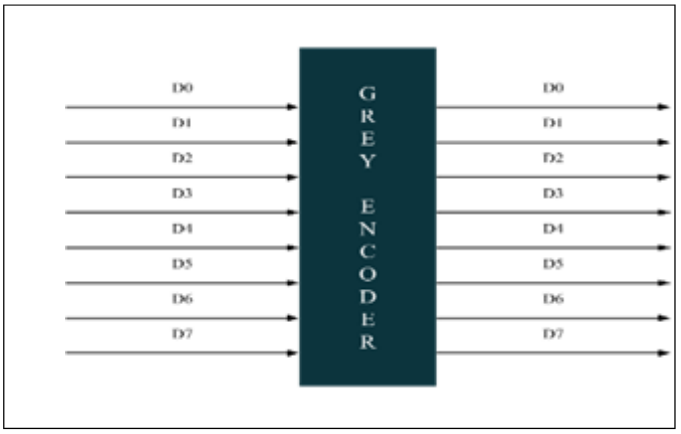
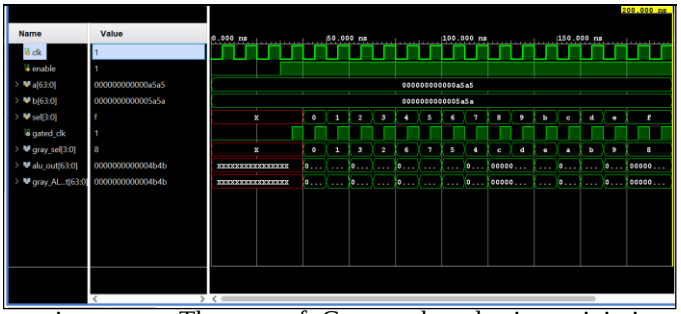


Fig.3: Gray Encoder (8 bit)

IV. RESULTS AND DISCUSSION

The simulation results demonstrate the expected functionality of the digital system, with proper clock synchronization and signal transitions. The clk signal maintains a stable waveform, while the enable signal remains high, ensuring continuous operation. The input values, a[63:0] = 0xA5A and b[63:0] = 0x5A5, remain constant, while the selection signal sel[3:0] cycles through different states, verifying multiple ALU operations. The gray_sel[3:0] follows a Gray code sequence, ensuring minimal bit transitions. Initially, the alu_out[63:0] and gray_ALU_out[63:0] outputs are undefined (XXXXXXXX), indicating a possible initialization delay. However, as the simulation progresses, both outputs stabilize to 0x4B4B, confirming correct computation.



transient state. The use of Gray code selection minimizes switching activity, which is beneficial for power efficiency and timing stability. The consistent final output values indicate that the ALU processes the selected operations correctly. These results validate the system's expected behavior, demonstrating accurate computation and controlled signal transitions in response to the input conditions.

The observed waveform indicates that the ALU operates as intended, processing inputs according to the selection signals. The **sel[3:0]** values transition sequentially, testing various ALU functions, while the **gray_sel[3:0]** ensures minimal bit transitions due to its Gray-coded nature. This transition technique is particularly useful in reducing dynamic power consumption and avoiding glitches in digital circuits. The ALU output remains undefined at the beginning but stabilizes as the simulation progresses, highlighting a potential delay in initialization or propagation time through the circuit. However, once stabilized, the outputs remain consistent, reinforcing the correctness of the ALU's operations.

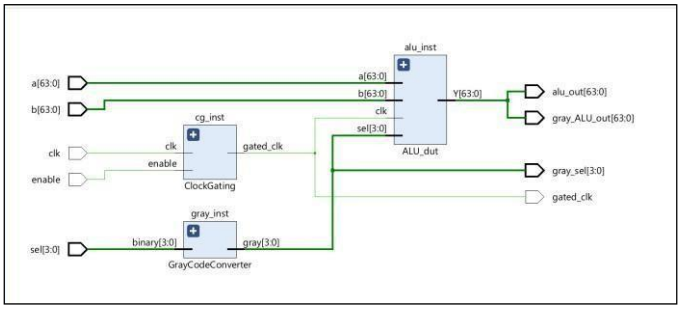


Fig.5: RTL Schematic Diagram

Additionally, the gated clocking mechanism appears to function correctly, as the gated_clk remains active throughout the simulation. This confirms that clock gating is implemented effectively, possibly reducing power consumption when needed. The final stable output values of alu_out[63:0] = 0x4B4B and gray_ALU_out[63:0] = 0x4B4B suggest accurate arithmetic or logical computations, aligning with expected results.

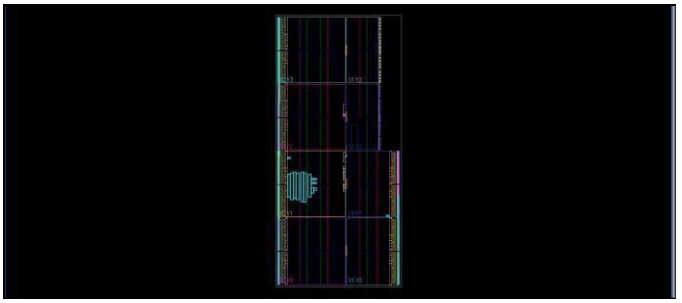


Fig.6: Implemented Design

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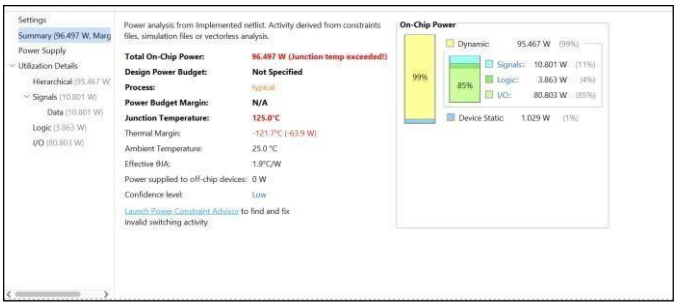

Fig.7: Power Consumption

V. CONCLUSION

The CGGC ALU architecture stands as a testament to the power of innovative design principles in addressing the challenges of power consumption in IoT applications. By combining clock gating and gray coding, this architecture achieves significant power savings while maintaining performance, making it a promising solution for the next generation of low-power, high- performance IoT devices. This development opens doors to a future where energy efficiency is not just a consideration but a fundamental building block for the ever-expanding world of the Internet of Things.

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